WE CLAIM:

1. A device for predistorting a digital symbol, comprising:

a processing module connected to an input parallel bit stream, wherein said processing module:

converts data bits of said input parallel bit stream into an input digital symbol;

applies a gain adjustment and a phase adjustment to said input digital symbol to produce a predistorted symbol; and

outputs quadrature components of said predistorted symbol.

2. The device of claim 1, further comprising:

a multi-bit buffer connected to an input serial bit stream; and

a clock that provides a clock signal to said multi-bit buffer, wherein:

said processing module reads said multi-bit buffer at said clock signal to convert said input serial bit stream to said input parallel bit stream.

3. The device of claim 1, wherein said processing module analyzes said data bits of said input parallel bit stream and determines the quadrature components (I_o; Q_o) of said input digital symbol.

4. The device of claim 1, wherein said processing module applies said gain adjustment and said phase adjustment to said input digital symbol to produce a predistorted symbol having a proper predistortion so that a received symbol matches said input digital symbol.

5. The device of claim 1, wherein said processing module decides which of a set of pre-set gain and phase adjustments to apply depending on a magnitude of said input digital symbol.

6. The device of claim 1, wherein said processing module applies said gain adjustment G_n and said phase adjustment Φn to said input digital symbol A_o to produce a predistorted symbol A_p according to:

$A_p = G_n (A_o) e^{j (\Phi n (Ao))}$.

7. The device of claim 1, further comprising:

a modulator wherein said processing module outputs said quadrature components of said predistorted symbol to said modulator and said modulator modulates an IF carrier by said quadrature components of said predistorted symbol.

8. A device for predistorting a digital symbol for modulating an RF signal, comprising:

a multi-bit buffer connected to an input serial bit stream and providing a parallel bit stream from said input serial bit stream;

a processing module connected to said input parallel bit stream, wherein said processing module:

converts data bits of said input parallel bit stream into an input digital symbol;

inputs a set of gain and phase adjustments that compensate for a channel distortion;

decides which of said set of gain and phase adjustments to apply depending on a magnitude of said input digital symbol;

applies a gain adjustment and a phase adjustment from said set of gain and phase adjustments to said input digital symbol to produce a predistorted symbol; and

outputs quadrature components of said predistorted symbol.

9. The device of claim 8, further comprising:

a clock that provides a clock signal to said multi-bit buffer, wherein:

said multi-bit buffer is an N-bit buffer and said clock operates at 1/N of the bit rate of said input serial bit stream; and

said processing module reads said multi-bit buffer at said clock signal to convert said input serial bit stream to said input parallel bit stream having width N.

10. The device of claim 8, wherein said processing module analyzes said data bits of said input parallel bit stream and determines the quadrature components (I_o ; Q_o) of said input digital symbol by mapping said data bits to an input symbol of a constellation map.

11. The device of claim 8, wherein said processing module applies said gain adjustment G_n and said phase adjustment Φ_n to the quadrature components (I_o ; Q_o) of said input digital symbol to produce a predistorted symbol having quadrature components (I_p ; Q_p) wherein:

$\sqrt{(I_p^2 + Q_p^2)} = G_n\sqrt{(I_o^2 + Q_o^2)}$ and

$\arctan(I_p / Q_p) = \Phi_n + \arctan(I_o / Q_o)$.

12. The device of claim 8, wherein said set of gain adjustments and phase adjustments that compensate for a channel distortion are calculated from amplifier gain curves to provide a proper predistortion so that a received symbol matches said input digital symbol.

13. The device of claim 8, wherein said set of gain adjustments and phase adjustments that compensate for a channel distortion are modified in real time using an adaptive loop to provide a proper predistortion so that a received symbol matches said input digital symbol.

14. The device of claim 8, further comprising:

a QPSK modulator wherein said predistorted symbol has quadrature components (I_p; Q_p) and said processing module outputs said quadrature components (I_p; Q_p) to said QPSK modulator and said QPSK modulator modulates an IF carrier by said quadrature components (I_p; Q_p).

15. A system for digitally predistorting and modulating an RF signal, comprising:

a multi-bit buffer connected to an input serial bit stream and providing a parallel bit stream from said input serial bit stream;

a processing module connected to said input parallel bit stream, wherein said processing module:

analyzes data bits of said input parallel bit stream and determines quadrature components (I_o; Q_o) of an input digital symbol by mapping said data bits to an input symbol of a constellation map;

inputs a set of gain adjustments and phase adjustments that compensate for a channel distortion;

decides which of said set of gain and phase adjustments to apply depending on a magnitude $\sqrt{(I_o^2 + Q_o^2)}$ of said input digital symbol;

applies a gain adjustment and a phase adjustment from said set of gain and phase adjustments to said input digital symbol to produce a predistorted symbol; and

outputs quadrature components (I_p; Q_p) of said predistorted symbol; and

a quadrature modulator wherein said processing module outputs said quadrature components (I_p; Q_p) to said quadrature modulator and said quadrature modulator modulates an IF carrier by said quadrature components (I_p; Q_p).

16. The system of claim 15, further comprising:

a clock that provides a clock signal to said multi-bit buffer, wherein:

said multi-bit buffer is an N-bit buffer and said clock operates at 1/N of the bit rate of said input serial bit stream, wherein said constellation map has m symbols and $N = \log_2(m)$; and

said processing module reads said multi-bit buffer at said clock signal to convert said input serial bit stream to said input parallel bit stream having width N so that said input digital symbol is an N-bit digital symbol.

17. The system of claim 15, wherein said processing module applies said gain adjustment G_n and said phase adjustment Φ_n to the quadrature components $(I_o; Q_o)$ of said input digital symbol A_o to produce a predistorted symbol A_p having quadrature components $(I_p; Q_p)$ wherein:

$\sqrt{(I_p^2 + Q_p^2)} = G_n\sqrt{(I_o^2 + Q_o^2)}$;

$\arctan(I_p / Q_p) = \Phi_n + \arctan(I_o / Q_o)$; and

$A_p = G_n (A_o) e^{j(\Phi n (Ao))}$.

18. The system of claim 15, wherein said set of gain adjustments and phase adjustments are provided in the form of a linear transformation so that a matrix multiplication is used to transform $(I_o; Q_o)$ to $(I_p; Q_p)$.

19. The system of claim 15, wherein said set of gain adjustments and phase adjustments that compensate for a channel distortion are calculated from amplifier gain curves to provide a proper predistortion so that a received symbol A matches said input digital symbol A_o according to:

$A= (G_d \cdot G_n)(A_o) e^{j(\Phi d + \Phi n)(Ao)}$.

20. The system of claim 15, wherein said set of gain adjustments and phase adjustments that compensate for a channel distortion are modified in real time using an adaptive loop to provide a proper predistortion so that a received

symbol matches said input digital symbol A_o according to:

$$A= (G_d \cdot G_n)(A_o)\, e^{j(\Phi d + \Phi n)(Ao)}.$$

21. The system of claim 15, further comprising:

a local oscillator, wherein:

said quadrature modulator is a QPSK modulator;

said local oscillator provides an IF carrier to said QPSK modulator;

said processing module outputs said quadrature components (I_p; Q_p) to said QPSK modulator; and

said QPSK modulator modulates said IF carrier by said quadrature components (I_p; Q_p) and outputs an m-QAM spectrum.

22. A satellite digital communications system, comprising:

a multi-bit buffer connected to an input serial bit stream and providing a parallel bit stream from said input serial bit stream;

a clock that provides a clock signal to said multi-bit buffer, wherein said multi-bit buffer is an N-bit buffer and said clock operates at 1/N of the bit rate of said input serial bit stream, wherein said multi-bit buffer is read at a transition of said clock signal to convert said input serial bit stream to said input parallel bit stream having width N so that an input digital symbol A_o of a constellation map is represented by N bits of said input serial bit stream; and wherein said constellation map has m symbols and $N = \log_2(m)$;

a processing module connected to said input parallel bit stream, wherein said processing module:

analyzes data bits of said input parallel bit stream and determines quadrature components (I_o; Q_o) of said input digital symbol A_o by mapping said data bits to an input symbol of a constellation map;

inputs a set of gain adjustments and phase adjustments that compensate for a channel distortion, wherein said set of gain adjustments and phase adjustments are provided in the form of a linear transformation so

that a matrix multiplication is used to transform quadrature components (I_o; Q_o) to quadrature components (I_p; Q_p) of a predistorted symbol A_p;

decides which of said set of gain and phase adjustments to apply depending on a magnitude $\sqrt{(I_o^2 + Q_o^2)}$ of said input digital symbol;

applies a gain adjustment G_n and a phase adjustment Φ_n from said set of gain and phase adjustments to said input digital symbol to produce a predistorted symbol; and

applies said gain adjustment G_n and said phase adjustment Φ_n from said set of gain and phase adjustments to said input digital symbol A_o to produce said predistorted symbol A_p according to:

$\sqrt{(I_p^2 + Q_p^2)} = G_n\sqrt{(I_o^2 + Q_o^2)}$;

$\arctan(I_p / Q_p) = \Phi_n + \arctan(I_o / Q_o)$; and

$A_p = G_n (A_o) e^{j (\Phi n (Ao))}$; and

outputs quadrature components (I_p; Q_p) of said predistorted symbol.

23. The system of claim 22, further comprising:

a quadrature modulator wherein said processing module outputs said quadrature components (I_p; Q_p) to said quadrature modulator; and

a local oscillator, wherein:

said local oscillator provides an IF carrier to said quadrature modulator; and

said quadrature modulator modulates said IF carrier by said quadrature components (I_p; Q_p) and outputs an m-QAM spectrum.

24. A method for digitally predistorting a digital signal, comprising:

converting data bits from a serial bit stream into an input digital symbol;

analyzing the input digital symbol bits to determine the quadrature components (I_o; Q_o) of the input digital symbol;

deciding which of a set of gain and phase adjustments G_n and Φ_n to apply to said input digital symbol;

performing a scaling and rotation transformation using gain and phase adjustments G_n and Φ_n on the quadrature components (I_o; Q_o) of the input digital symbol; and

providing quadrature components (I_p; Q_p) for a predistorted symbol.

25. The method of claim 24 further comprising a step of:

providing a said set of gain and phase adjustments G_n and Φ_n calculated from amplifier gain curves for compensating for a channel distortion.

26. The method of claim 24 further comprising a step of:

providing a said set of gain and phase adjustments G_n and Φ_n modified in real time using an adaptive loop for compensating for a channel distortion.

27. The method of claim 24 further comprising a step of:

providing a said set of gain and phase adjustments G_n and Φ_n in the form of a linear transformation so that a matrix multiplication is used to transform (I_o; Q_o) to (I_p; Q_p).

28. The method of claim 24 further comprising a step of:

converting a serial bit stream to an N-bit parallel bit stream, convert N of the data bits to an input digital symbol.

29. The method of claim 24 further comprising a step of:

modulating an RF carrier by said predistorted symbol having quadrature components (I_p; Q_p).